

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended): A method for recovering a clock signal from an input data signal in a telecommunications system, the method comprising ~~the steps of:~~

comparing the input data signal with a recovered clock signal in order to control said recovered clock signal generation; ~~and~~

generating a plurality of delayed clock signals, obtained by multi-delaying at least a reference signal, said delayed clock signals being phase-shifted with respect to each other;

selecting the recovered clock signal among said delayed clock signals; and

employing a number of delayed signals, such that the sum of the shifts associated with such delayed signals covers the bit period of the input data signal;

wherein said delayed clock signals show a phase shift with respect to each other, that is nominally constant in time, ~~and wherein it further comprises the step of selecting the recovered clock signal among said delayed clock signals.~~

2. (Canceled)

3. (Currently Amended): ~~Method~~The method according to claim 21, ~~wherein it~~
further ~~comprises~~comprising the step of dynamically changing the number of delayed signals by
comparing the bit period with the shift sum.

4. (Currently Amended): ~~Method~~The method according to claim 3, wherein the shift
between each adjacent pair of delayed signals is nominally equal.

5. (Currently Amended): ~~Method~~The method according to claim 3, ~~wherein it~~
~~comprises the step of~~further comprising obtaining said plurality of delayed clock signals by
multi-delaying a single sole reference signal.

6. (Currently Amended): ~~Method~~The method according to claim 4, ~~wherein it~~
further ~~comprises the step of~~comprising selecting a first recovery signal and a second recovery
signal before selecting the recovery clock signal.

7. (Currently Amended): ~~Method~~The method according to claim 5, ~~wherein it~~
further ~~comprises the step of~~comprising switching between said first recovery signal and said
second recovery signal for selecting the recovery clock signal.

8. (Currently Amended): ~~Method~~The method according to claim 5, ~~wherein it~~
~~comprises the step of~~further comprising shifting the first recovery signal and the second recovery
signal by one time interval.

9. (Currently Amended): ~~Method~~The method according to claim 6, ~~wherein it~~
~~comprises the step of~~further comprising shifting the first recovery signal and the second recovery
signal by one time interval.

10. (Currently Amended): ~~Method~~The method according to claim 5, ~~wherein it~~
further ~~comprises the step of~~comprising providing enabling signals for activating switching
between said first recovery signal and said second recovery signal.

11. (Currently Amended): ~~Method~~The method according to ~~any of claims~~claim 1,
~~wherein it further comprises the step of~~comprising comparing the input data signal with the
recovered clock signal, by using the comparison of several phases of at least one of the input data
signal ~~and/or of~~and the recovered clock signal, so as to obtain a plurality of samples for each
sampling cycle.

12. (Currently Amended): ~~Method~~The method according to claim 10, ~~wherein it~~
further ~~comprises the step of~~comprising filtering the output of the comparison operation.

13. (Currently Amended): ~~A Circuit~~circuit for recovering a clock signal from an input data signal in a telecommunications network, ~~the circuit comprising:~~

a generating means configured to generate a recovery clock signal; and

a phase comparator configured to comparingcompare the input data signal phase and the recovery clock signal phase for supplying a phase information, which controls said generating means of said recovery clock signal;

wherein said generating means ~~comprise~~further comprises a delay line having a plurality of taps for generating a plurality of delayed signals, and

wherein the sum of the shifts associated with such delayed signals covers the bit period of the input data signal.

14. (Currently Amended): ~~Circuit~~The circuit according to claim 13, wherein said generating means ~~comprise~~comprises a selection means of the recovered clock signal.

15. (Currently Amended): ~~Circuit~~The circuit according to claim 13, further comprising a selection means, wherein said selection means ~~comprise~~comprises a first-selection block for selecting a first recovery signal and a second recovery signal from the plurality of delayed signals, and further ~~comprise~~comprises a second-switch block for switching between said first recovery signal and said second recovery signal.

16. (Currently Amended): ~~Circuit~~ The circuit according to claim 14, wherein said selection means ~~comprise~~ further comprises, ~~moreover~~, a control ~~logies~~ logic driving ~~the a first~~ selection block and ~~the a second~~ switch block according to the phase information supplied by the phase comparator.

17. (Currently Amended): ~~Circuit~~ The circuit according to claim 15, wherein said control ~~logies~~ logic comprises a filter for filtering the phase information.

18. (Currently Amended): ~~Circuit~~ The circuit according to claim 15, wherein said control ~~logies~~ logic comprises a logic machine issuing selection signals and enable signals according to the phase information.

19. (New): A circuit for recovering a clock signal from an input data signal in a telecommunications network, comprising:

a generating means configured to generate a recovery clock signal;

a phase comparator configured to compare the input data signal phase and the recovery clock signal phase for supplying a phase information, which controls said generating means of said recovery clock signal;

a selection means;

wherein said generating means comprises a delay line having a plurality of taps for generating a plurality of delayed signals;

wherein said selection means comprises a selection block for selecting a first recovery signal and a second recovery signal from the plurality of delayed signals, and further comprises a switch block for switching between said first recovery signal and said second recovery signal.

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20. (New): The circuit according to claim 19, wherein said control logic comprises a filter for filtering the phase information.

21. (New): The circuit according to claim 19, wherein said control logic comprises a logic machine issuing selection signals and enable signals according to the phase information.
